REMARKS / ARGUMENTS

Claims 1-24 remain pending.

35 U.S.C. §103

Claims 1-9 and 22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thompson et al, U.S. Patent No. 6,510,309 (Thompson) in view of Tanaka (JP 57-43453) and Matsubara (JP 02-142185). Claims 10-21, 23 and 24 are rejected under §103(a) as being unpatentable over the Thompson, Matsubara and Tanaka combination in view of Lysejko et al, U.S. Patent No. 6,298,246 (Lysejko). Claim 14 is rejected under §103(a) as being unpatentable over the Thompson, Matsubara and Tanaka combination in view of Yamamoto et al, U.S. Patent No. 6,308,047 (Yamamoto). Reconsideration of the rejections is respectfully requested.

Applicants' position with respect to the differences between the invention as claimed in claims 1-24 with respect to the Thompson, Tanaka, Lysejko and Yamamoto references is of record in the Amendment filed December 7, 2004. The Examiner has added the reference of Matsubara in finally rejecting the claims. Accordingly, Applicants respond to the rejections by emphasizing that the addition of Matsubara to the Thompson and Tanaka references does not render the invention of claims 1-9 and 22 unpatentable, and further the addition of Matsubara to the Thompson, Tanaka and Lysejko references does not render claims 10-13, 15-21, 23

and 24 unpatentable. Further. the Yamamoto reference is also unable to overcome the deficiencies of Thompson, Tanaka, Matsubara and Lysejko in regard to the rejection of claim 14.

The Examiner recognizes that the combination of Tanaka and Thompson does not teach a wireless communication system in which the wirings are arranged such that none of the wirings are arranged to traverse the wirings respectively connected between a first electrode terminal and a first electrode of the transistor, a second electrode terminal and a second electrode of the transistor, and between a third electrode terminal and a control electrode of the transistor, as set forth in independent claim 1. Further, the combination of Tanaka and Thompson does not teach that the wirings in each of the signal processing integrated circuits are arranged such that none traverse the wirings respectively connected between the first ones of the electrode terminals and the first electrodes of the transistors, between the second ones of the electrode terminals and the second electrodes of the transistors, and between the third ones of the electrode terminals and the control electrodes of the transistors, as set forth in independent claim 10. Accordingly, Matsubara is relied upon in the Office Action for teaching wirings, wherein none of the wirings are arranged to traverse the wirings respectively connected between the first, second and third electrode terminals and the corresponding first, second and control electrodes of the transistor as set forth in Figures 1, 5 and 6 of the reference. However, Applicants traverse the conclusion made in the Office Action from the

disclosure of the reference that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the teachings of Matsubara to the system of Thompson and Tanaka in order to reduce parasitic inductance in a wireless IC.

Matsubara discloses an arrangement of pads and transistors, without relating the disclosure to a wireless communication system. Further, the reference does not mention reducing unnecessary parasitic inductance. Rather, the pads disclosed by Matsubara are only used for testing the transistor. In detail, Matsubara relates to a technique for determining the quality of a transistor 3 using tests to determine whether or not the transistor passes or fails. The tests involve placement of probes or test rods 14 and 15 on probe pads 10, 11 and 12. The test rods 14 and 15 are spaced apart a predetermined distance and applied in the different configurations shown in Figures 2-4 of the reference. In the prior art to Matsubara, when using a 2-probe tester, the interval or distance between the probes needed to be changed for each test (see Figures 7-9 of Matsubara). By the invention of Matsubara, the placement of the probe pads enables a fixed interval or distance to be maintained between the probes or test rods 14 and 15 with respect to the probe pads, and therefore the different tests can be conducted without adjusting the distance between the probes or test rods 14 and 15. This enables efficient testing of the transistor.

Matsubara does not disclose the arrangement of pads (terminals) and transistors on a semiconductor chip, or the connection of a control electrode, first

electrode and second electrode (of the transistor) to electrode terminals (pads) through wirings that are relatively short, as set forth in amended claims 1 and 10. See page 24, lines 8-18 of the specification for the description of the arrangement of the pads (terminals) 101-103 and the short wirings between the terminals or pads and the electrodes of the transistor. The invention of claims 1 ands 10 includes a main surface of a semiconductor chip provided with a plurality of the electrode pads (terminals) along an edge portion thereof in combination with relatively short wirings between the pads or terminals and the electrodes of the transistor, which is not disclosed by Matsubara. Further, the electrode terminals of the invention are not provided for testing, as they are in Matsubara. The arrangement set forth in the claimed combination, therefore, is not equivalent to that shown in Matsubara, and therefore the combination of Thompson, Tanaka, Lysejko and Matsubara does not teach the claimed arrangement of wirings that enables a reduction in parasitic inductance as is achieved by the wireless communication system claimed in the present invention.

Although Applicants have argued the patentability of independent claims 1 and 10 over the combination of references relied upon in the 35 U.S.C. §103(a) rejections, Applicants respectfully assert that the remainder of the claims, which are dependent claims, are patentable over the references relied upon in the rejections, and the remainder of the art of record, at least for being dependent from an independent claim asserted to be allowable for the foregoing reasons.

CONCLUSION

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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